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H04L 1/00, G11B 20/18

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H4P PEX

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(58) Field of search
UK CL (Edition L) H4P PEM PEP PEX
INT CL[5] G11B 20/18, H04L 1/00
WPI

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(54) Audio data processing system

(57) An audio data processing system includes an interpolation circuit to correct for so-called double errors in successive digital audio samples: 64-Bit parallel samples of an audio signal, typically comprising four simultaneous audio channels for a sattelite t.v. transmission, are checked and corrected for single bit errors by a Bose-Chaudhuri-Hocquenghem (BCH) circuit (not shown). Samples containing double bit errors, which cannot be corrected by the BCH circuit, are replaced by average values. When a sample containing a double error is detected, it is substituted by an average value based on the non-erroneous samples preceding and following the detected erroneous sample (Fig. 1A). When a succession of samples are detected to contain double errors, the last non-erroneous sample value is used as a substitution for the erroneous samples except for the last sample in the succession, which is substituted by the aforesaid average value (Fig. 1B).

FIG. 1A

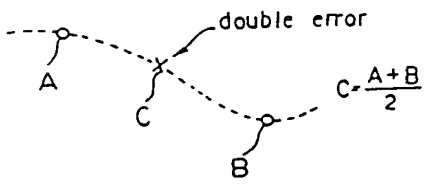
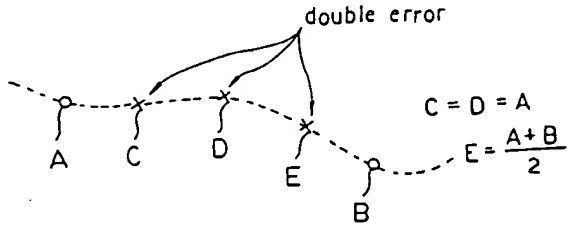


FIG. 1B



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WPI

S2

(54) Audio data processing system

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FIG. 1A

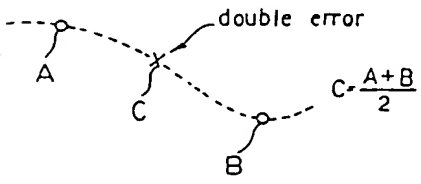
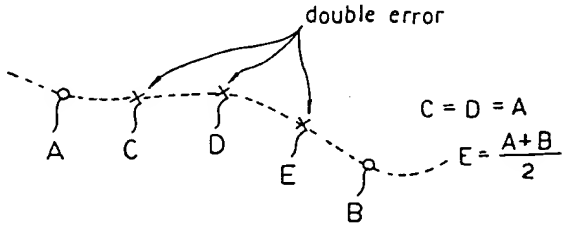


FIG. 1B



GB 2 266 435 A

FIG. 1A

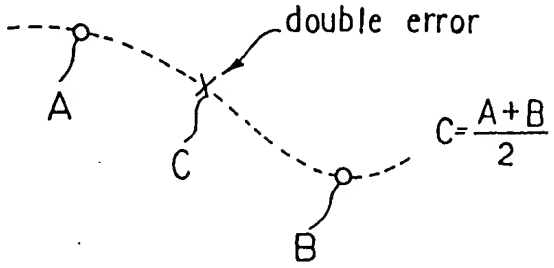


FIG. 1B

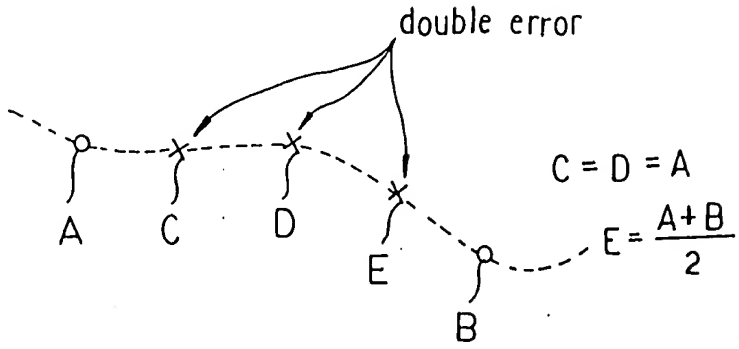


FIG. 2

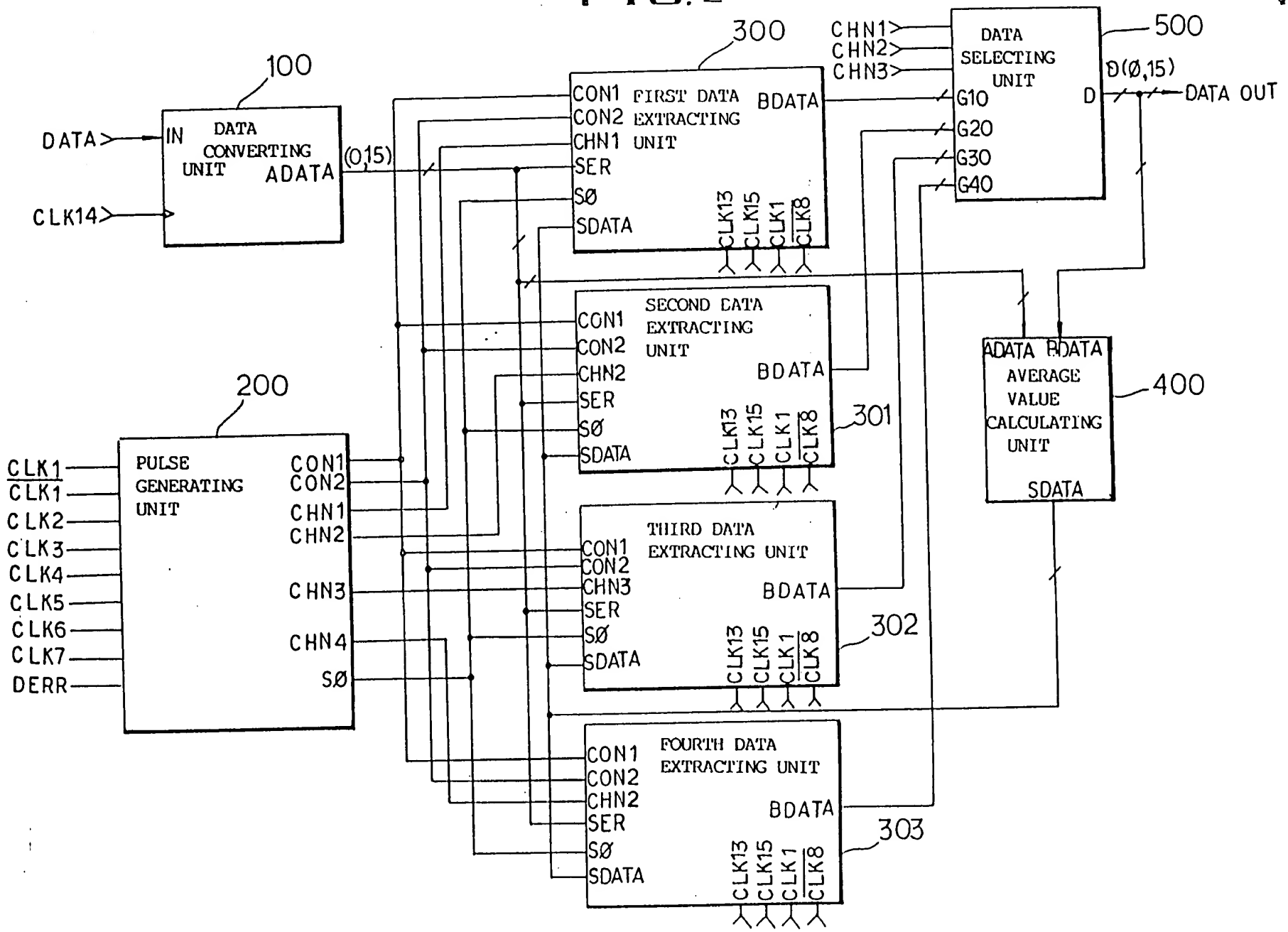

100
DATA
IN
DATA CONVERTING UNIT
ADATA
CLK14
(0,15)
200
PULSE GENERATING UNIT
CLK1
CLK1
CLK2
CLK3
CLK4
CLK5
CLK6
CLK7
DERR
CON1
CON2
CHN1
CHN2
CHN3
CHN4
SØ
300
CON1 FIRST DATA
CON2 EXTRACTING
CHN1 UNIT
SER
SØ
SDATA
BDATA
CLK13
CLK15
CLK1
CLK8
SECOND DATA EXTRACTING UNIT
301
THIRD DATA EXTRACTING UNIT
302
FOURTH DATA EXTRACTING UNIT
303
CHN1
CHN2
CHN3
DATA SELECTING UNIT
500
G10
G20
G30
G40
D
D(Ø,15)
DATA OUT
ADATA BDATA
AVERAGE VALUE CALCULATING UNIT
400
SDATA

FIG.3

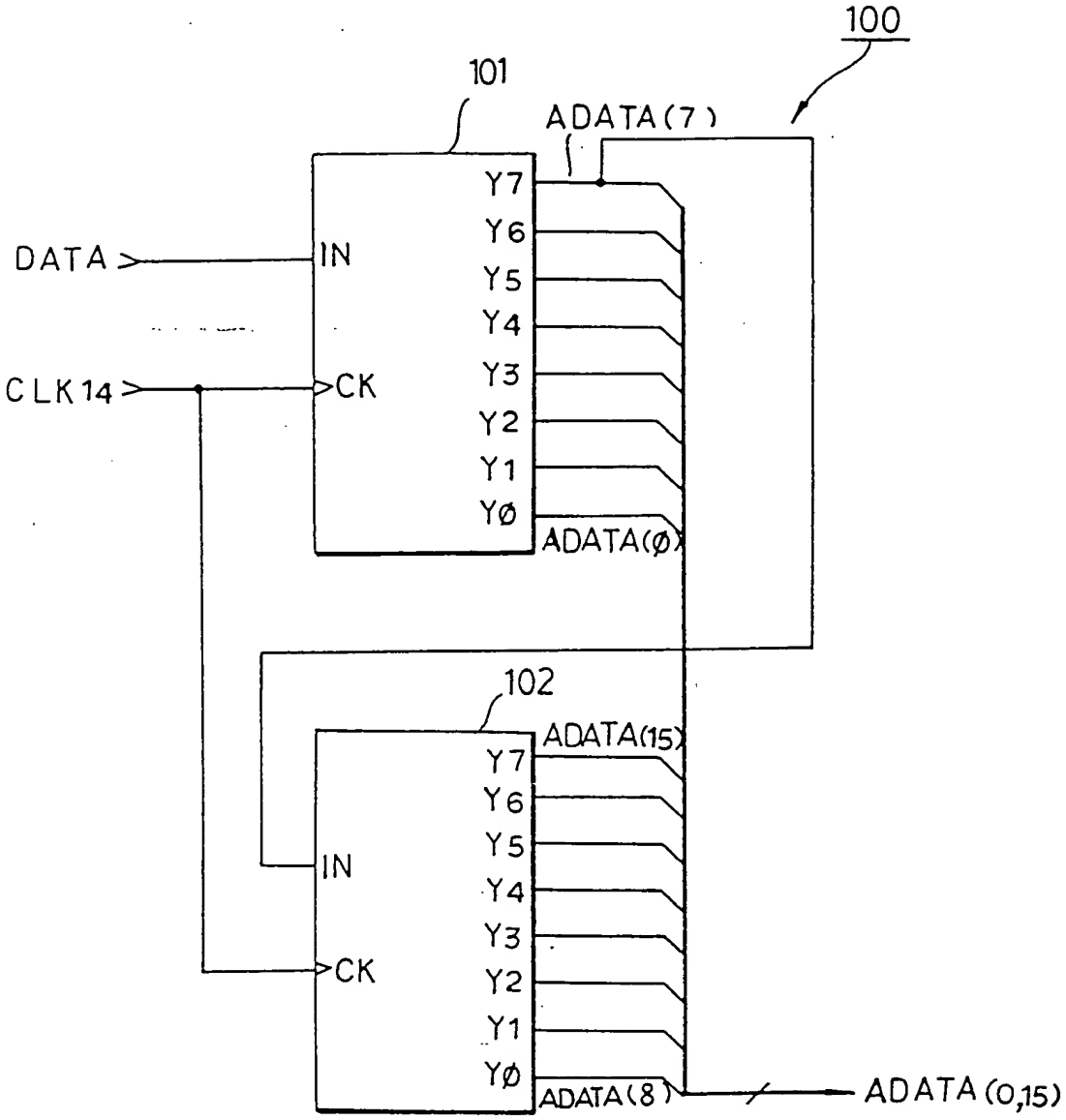

100
101
ADATA(7)
Y7
Y6
Y5
Y4
Y3
Y2
Y1
YØ
DATA
IN
CLK14
CK
ADATA(Ø)
102
ADATA(15)
Y7
Y6
Y5
Y4
Y3
Y2
Y1
YØ
IN
CK
ADATA(8)
ADATA(0,15)

FIG. 4A

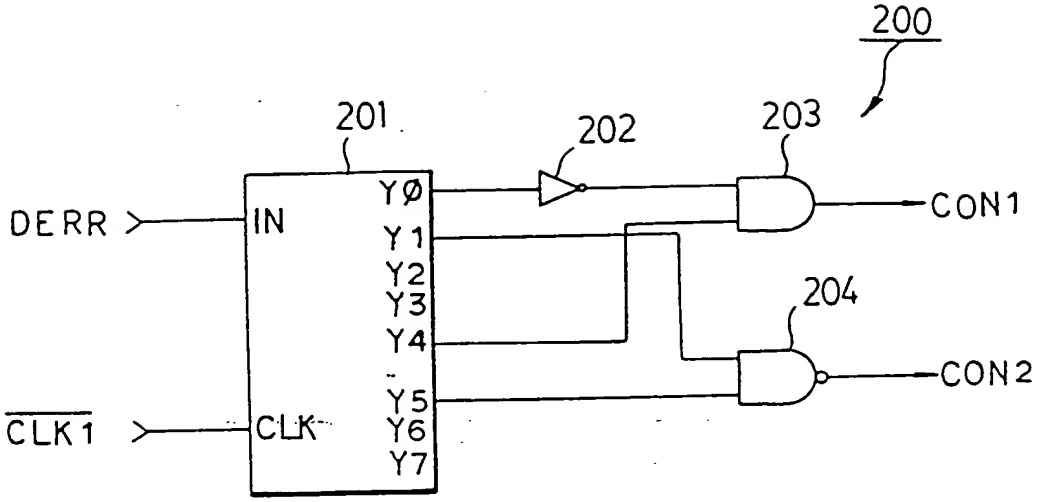


FIG. 4B

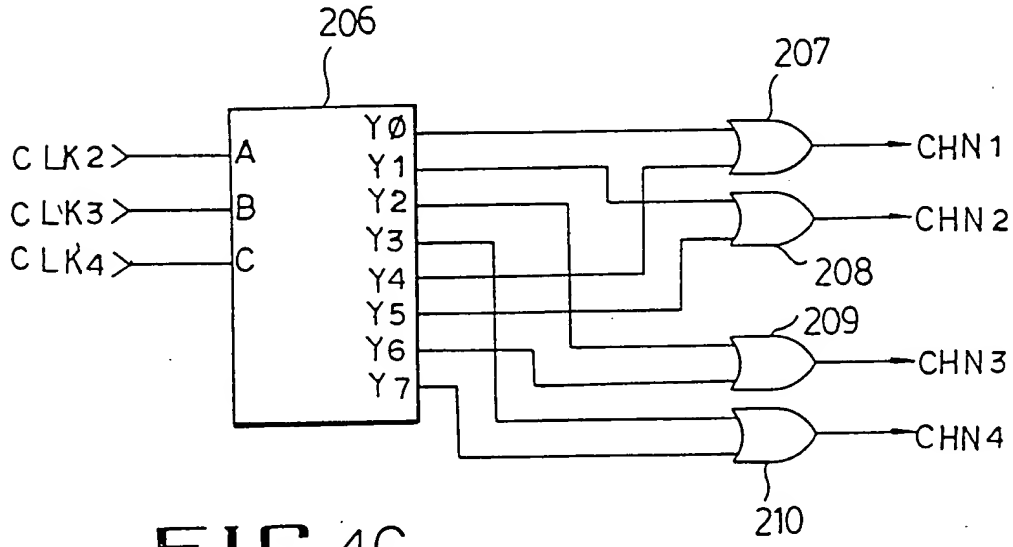


FIG. 4C

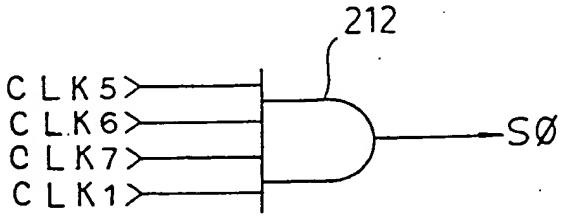


FIG.5

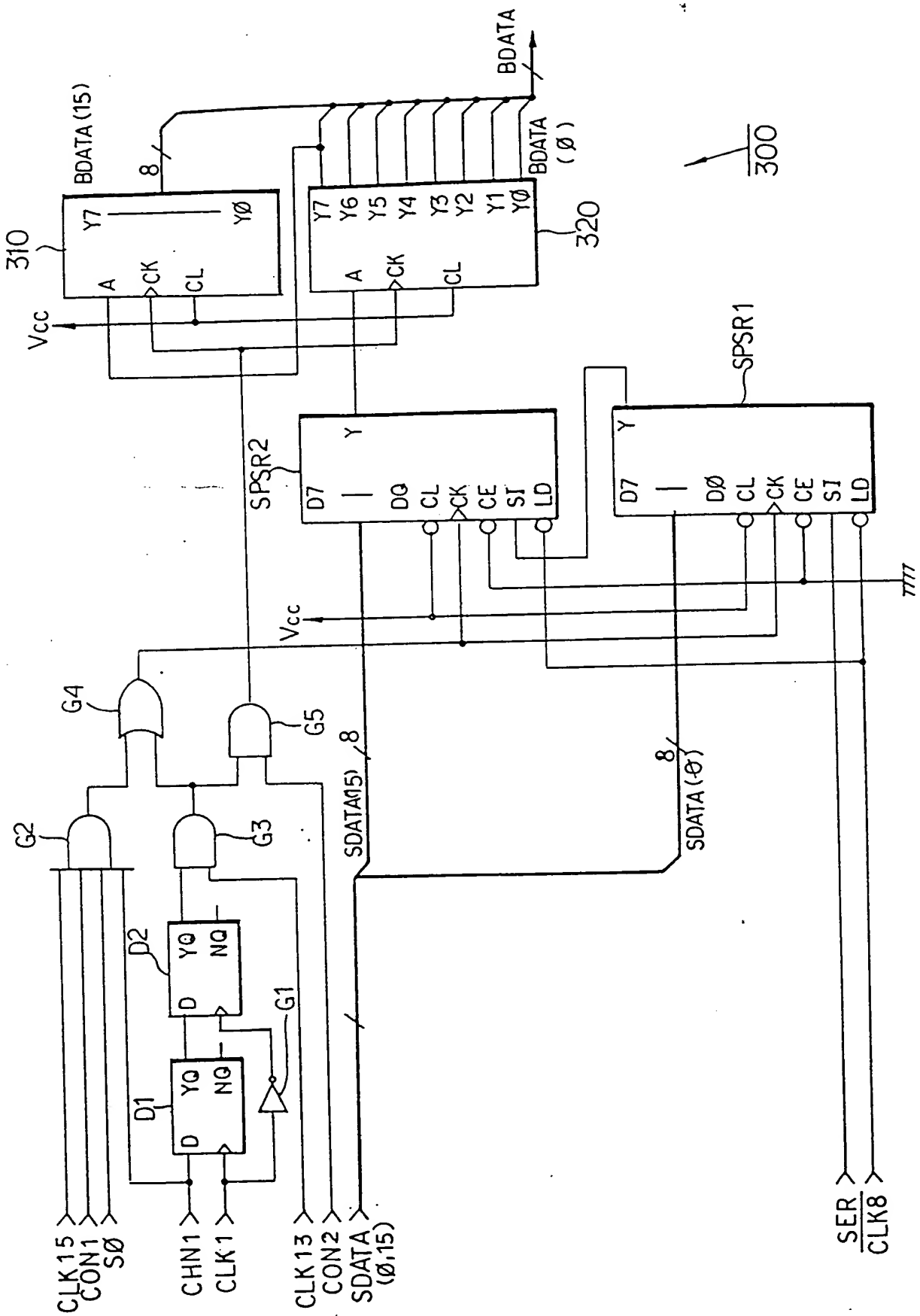

BDATA
BDATA (15)
BDATA (Ø)
8
310
320
300
Y7
YØ
A
CK
CL
Y7 Y6 Y5 Y4 Y3 Y2 Y1 YØ
Vcc
SPSR2
SPSR1
D7
Y
DQ
DØ
CL
CK
CE
SI
LD
G4
G5
G2
G3
G1
D2
D1
YQ
NQ
D
SDATA(15)
SDATA(Ø)
CLK15
CON1
SØ
CHN1
CLK1
CLK13
CON2
SDATA (Ø,15)
SER
CLK8

FIG. 6

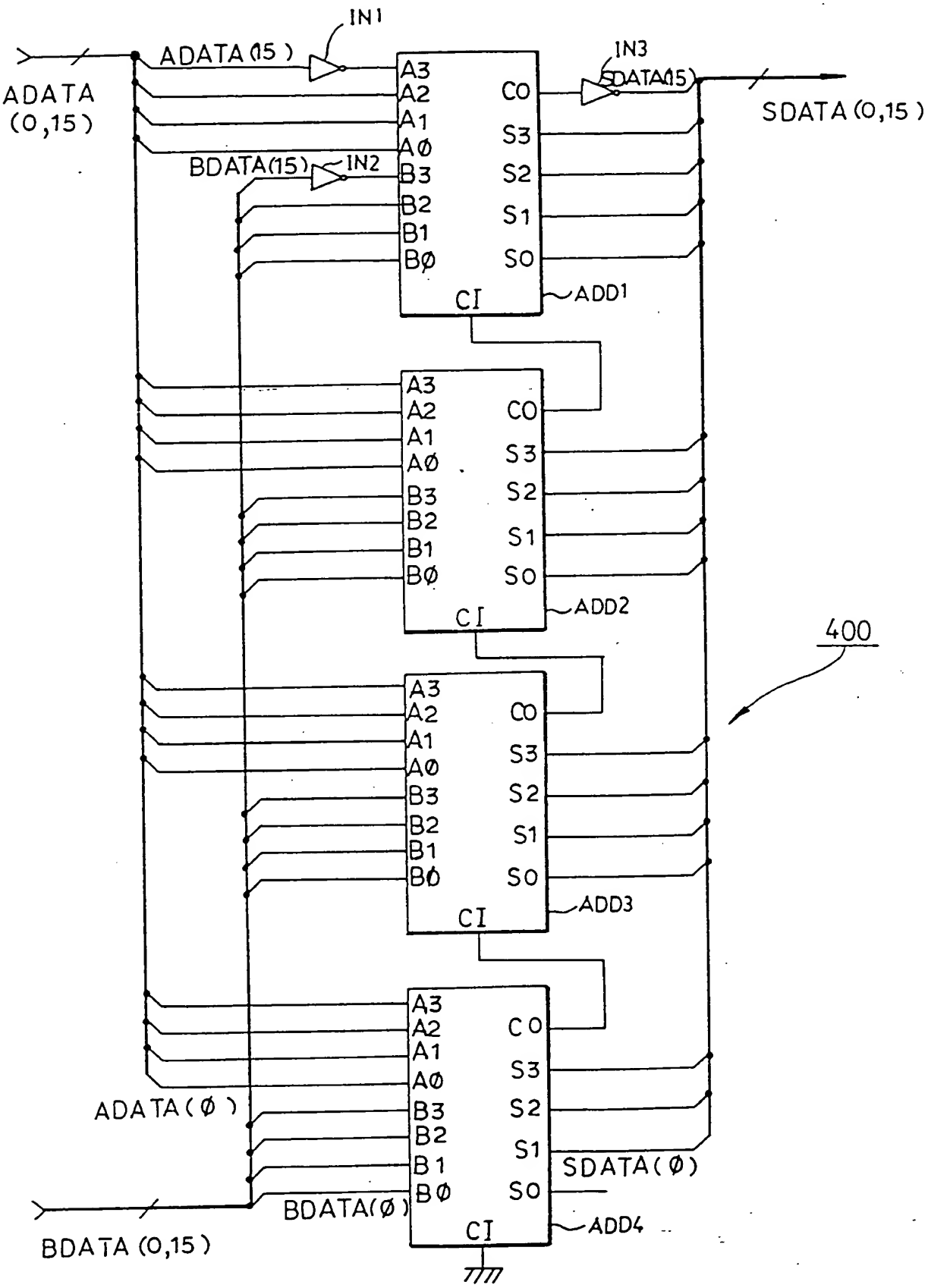

IN1
ADATA (15)
ADATA (0,15)
IN3
SDATA(15)
SDATA (0,15)
BDATA(15)
IN2
A3
A2
A1
AØ
B3
B2
B1
BØ
CO
S3
S2
S1
SO
CI
ADD1
ADD2
ADD3
ADD4
400
ADATA (Ø)
BDATA (0,15)
BDATA(Ø)
SDATA(Ø)

FIG. 7

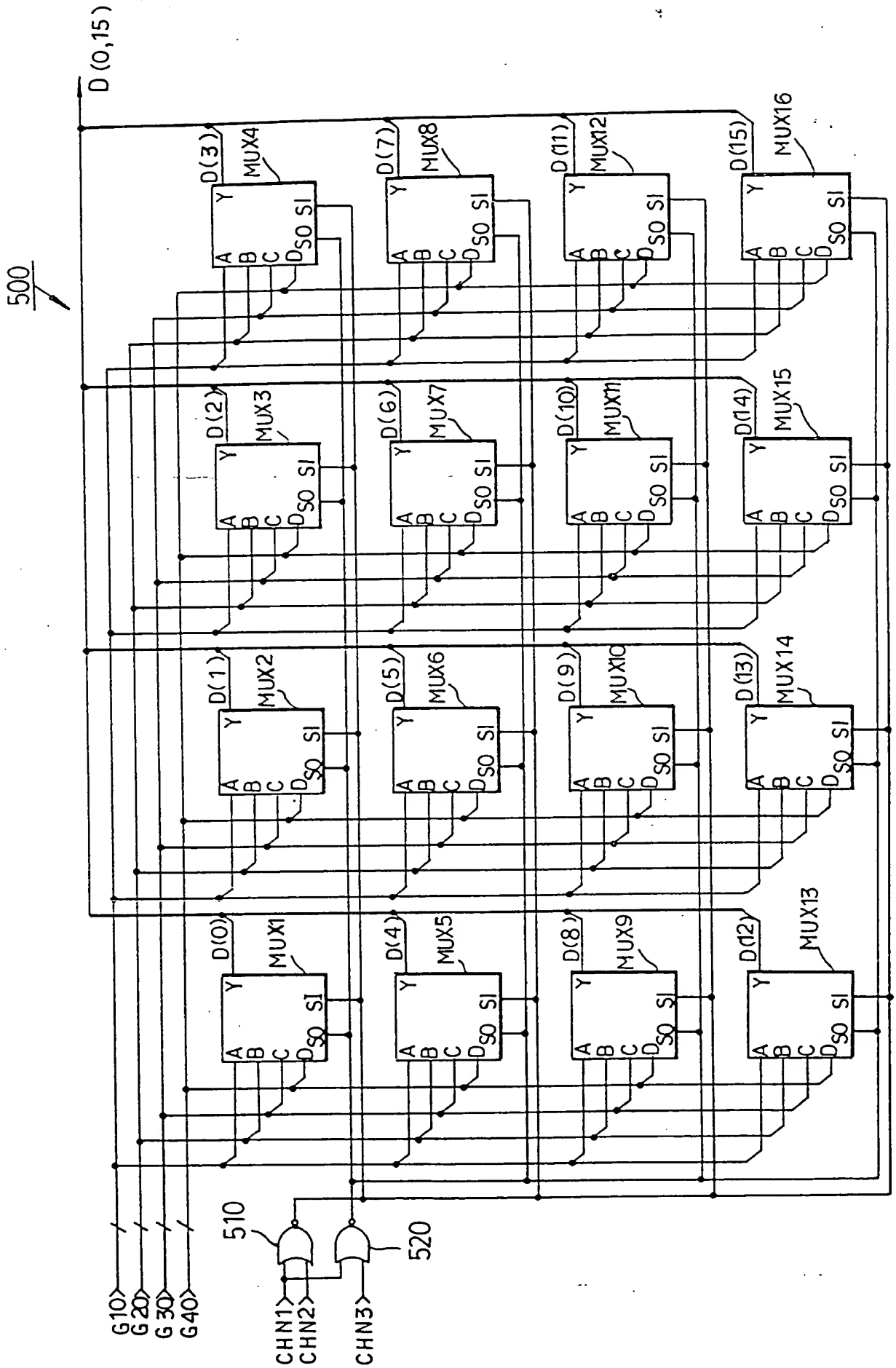

500
D(0,15)
MUX1
MUX2
MUX3
MUX4
MUX5
MUX6
MUX7
MUX8
MUX9
MUX10
MUX11
MUX12
MUX13
MUX14
MUX15
MUX16
D(0)
D(1)
D(2)
D(3)
D(4)
D(5)
D(6)
D(7)
D(8)
D(9)
D(10)
D(11)
D(12)
D(13)
D(14)
D(15)
A
B
C
D
Y
SO
SI
510
520
G10
G20
G30
G40
CHN1
CHN2
CHN3

FIG. 8

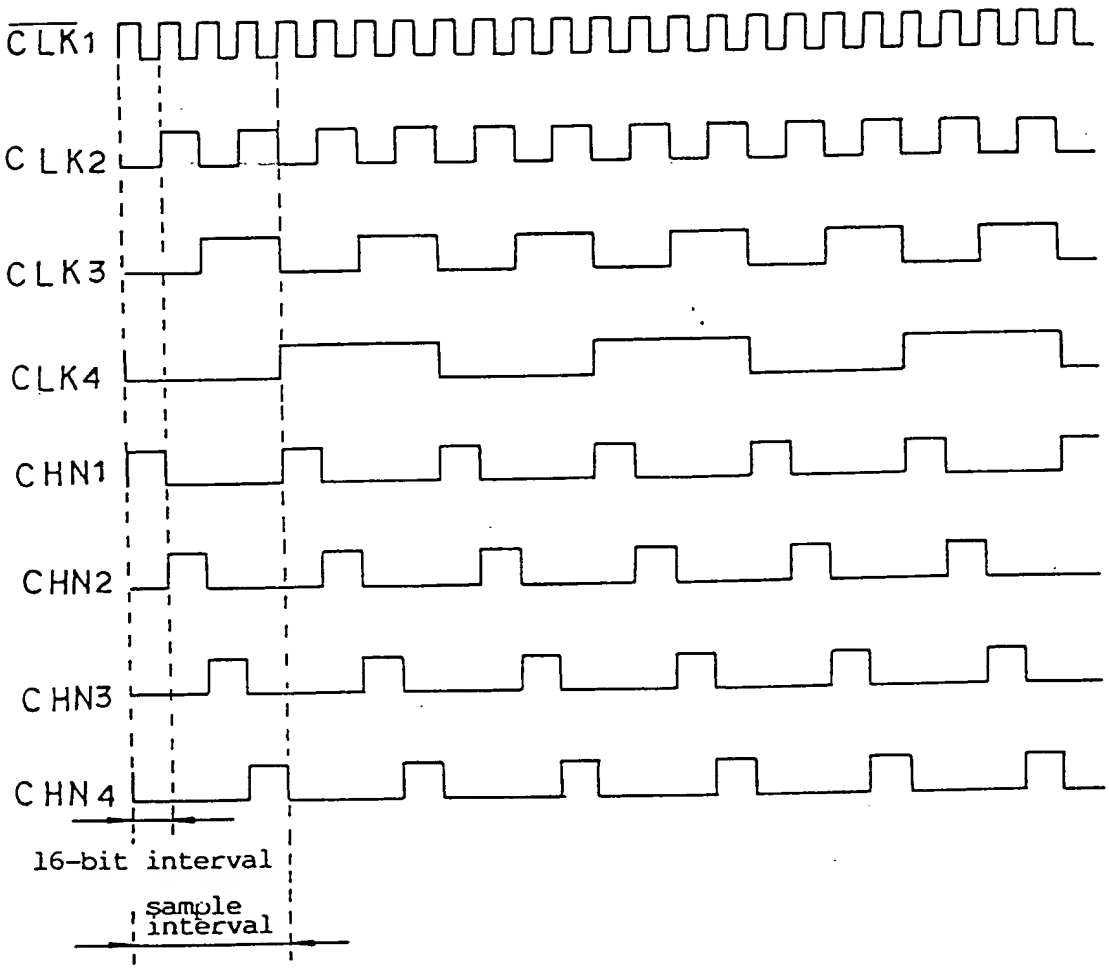

CLK1
CLK2
CLK3
CLK4
CHN1
CHN2
CHN3
CHN4
16-bit interval
sample interval

FIG. 9

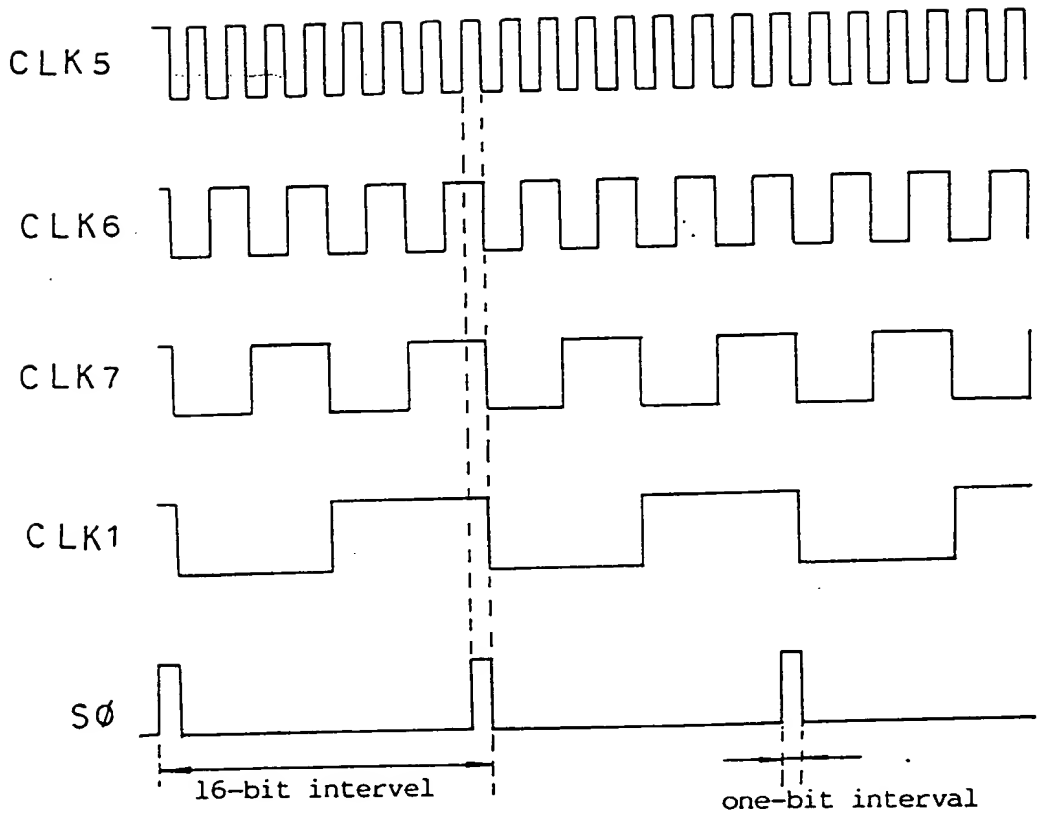


FIG.10

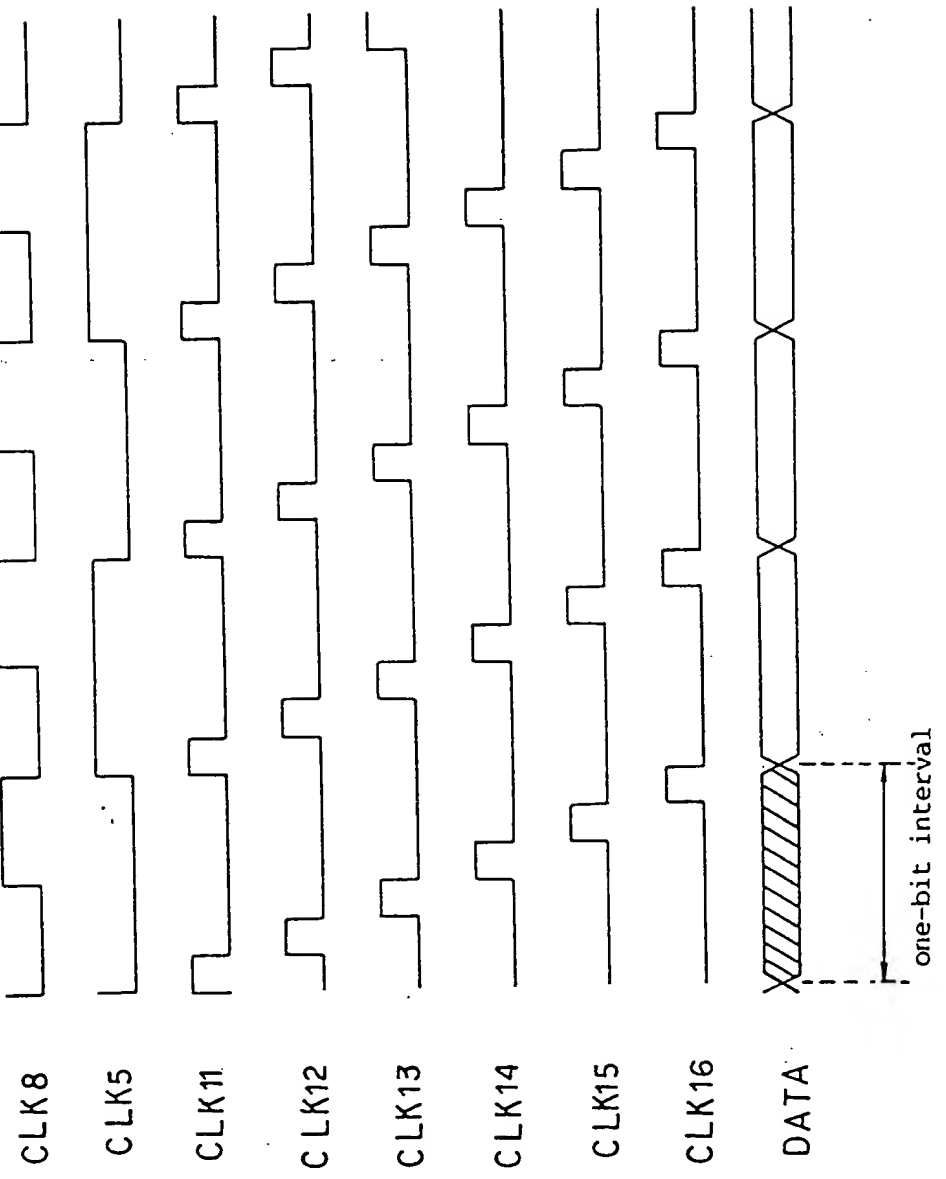

CLK8
CLK5
CLK11
CLK12
CLK13
CLK14
CLK15
CLK16
DATA
one-bit interval

FIG. 11

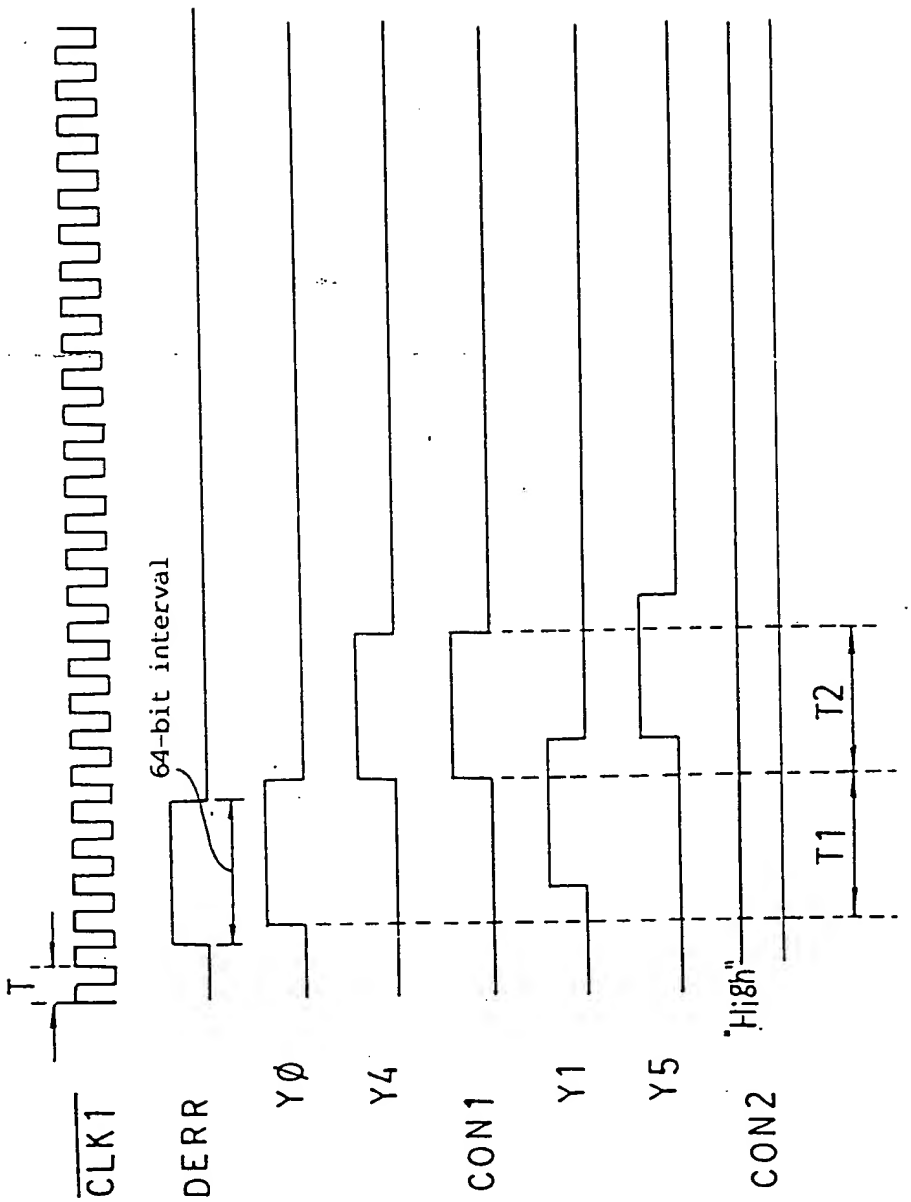


FIG.12

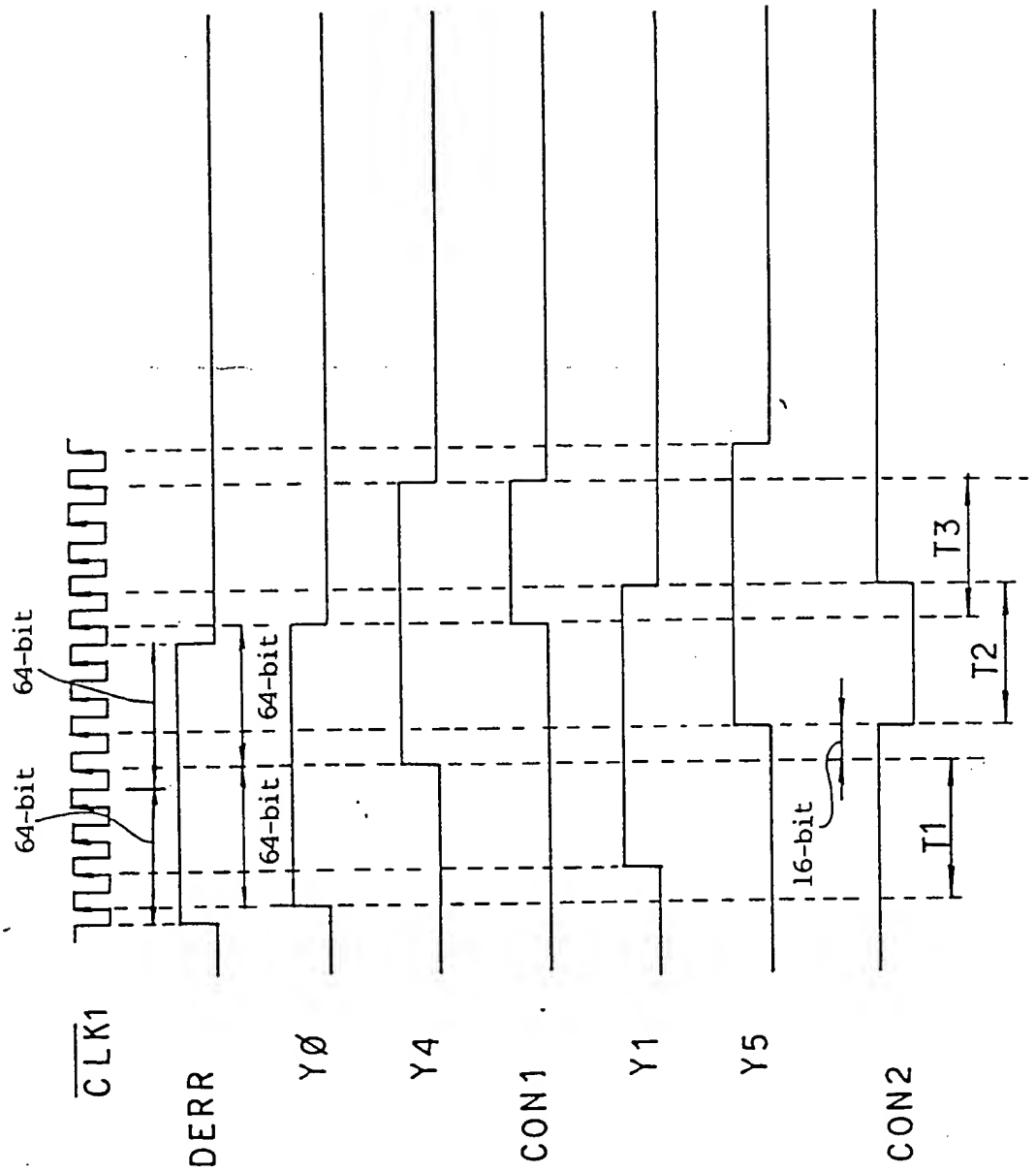

64-bit
64-bit
64-bit
64-bit
16-bit
T1
T2
T3
CLK1
DERR
YØ
Y4
CON1
Y1
Y5
CON2

FIG.13A

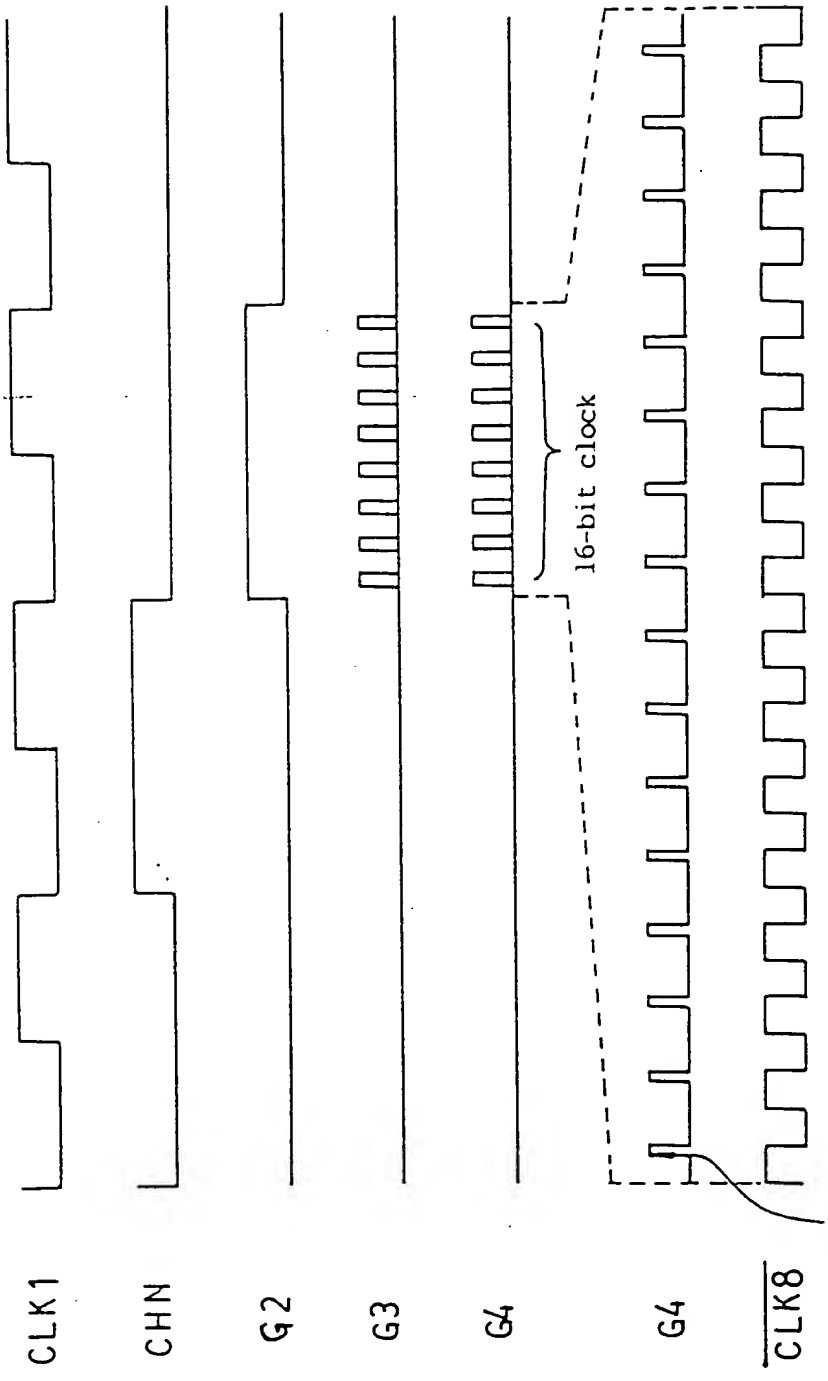


FIG. 13B

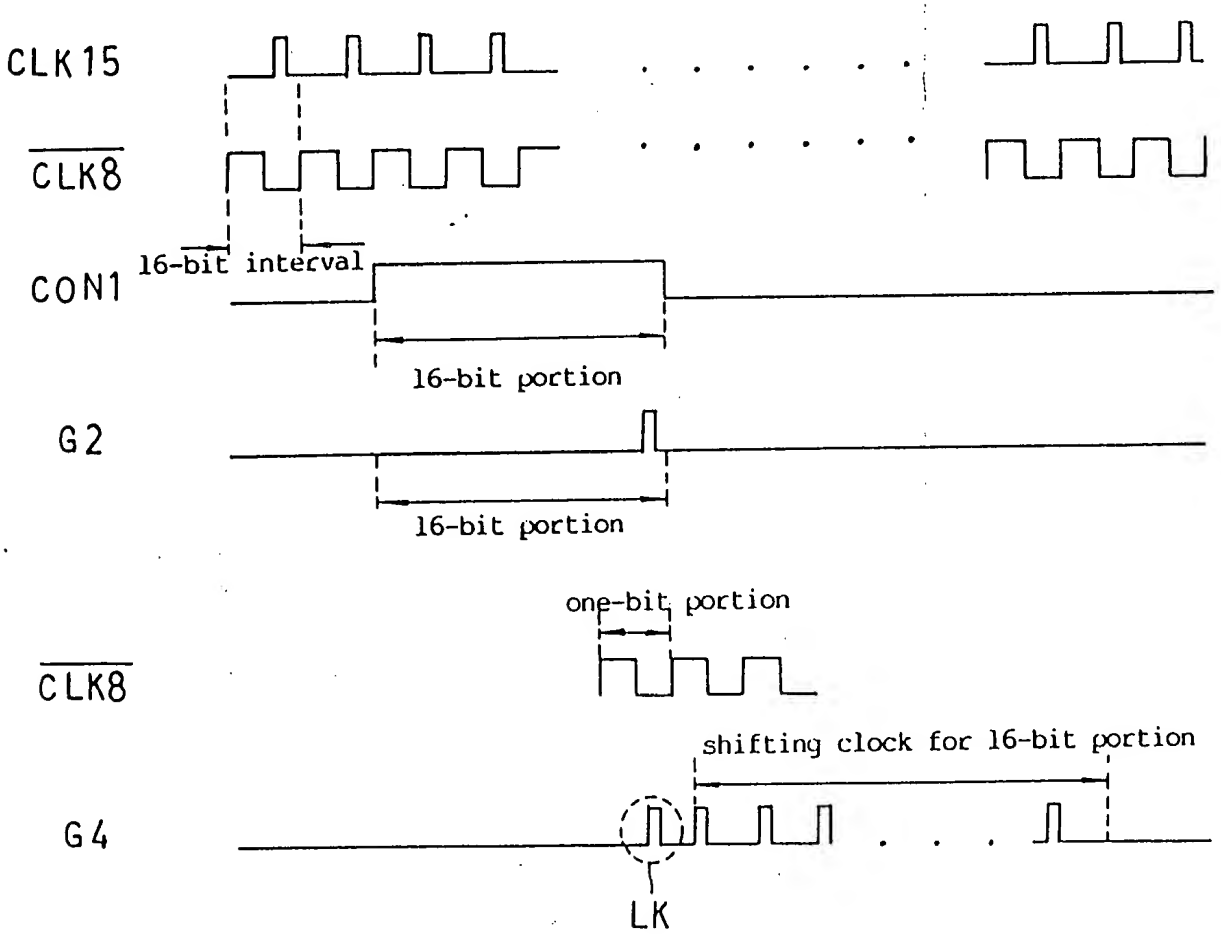
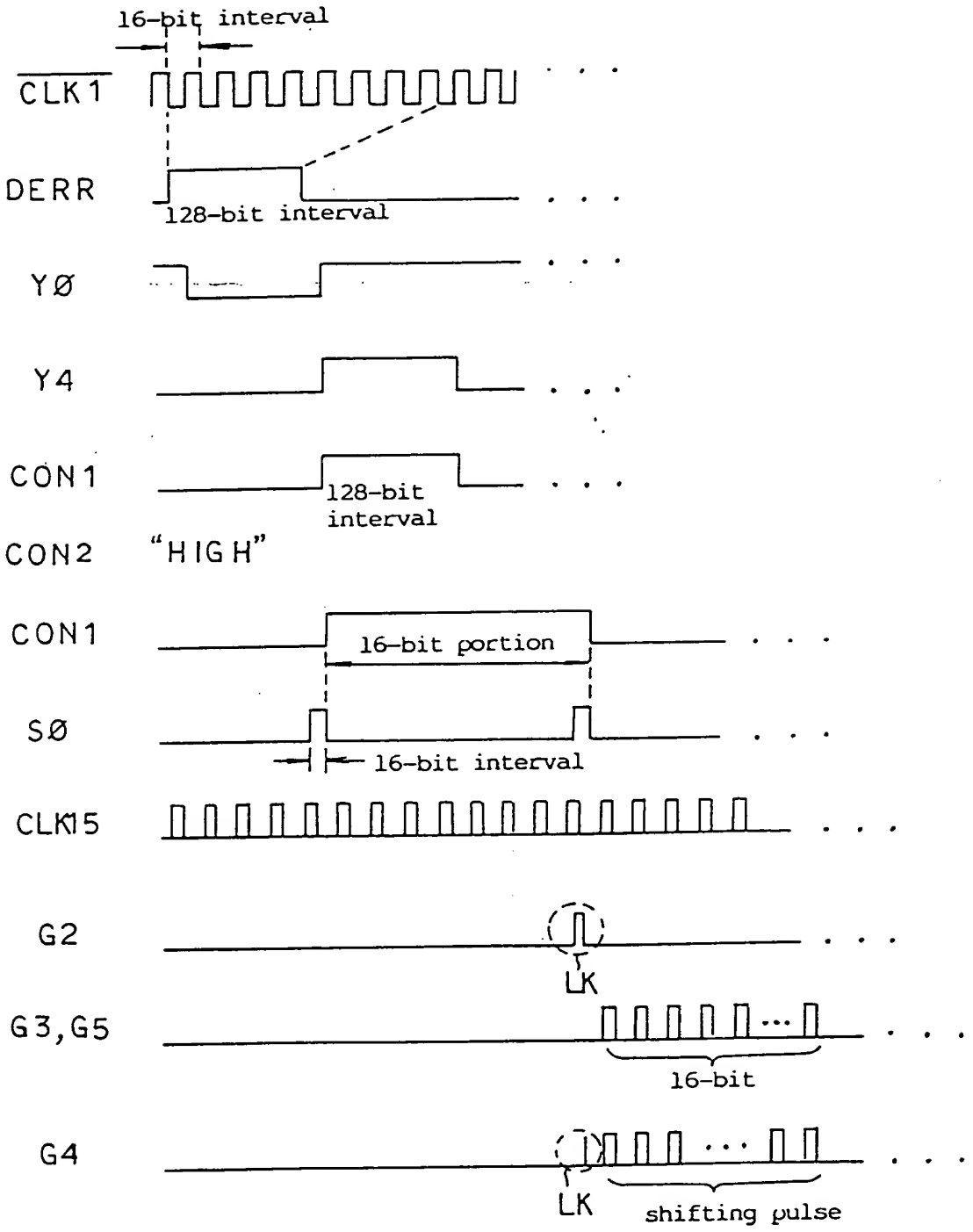

CLK15
CLK8
16-bit interval
CON1
16-bit portion
G2
16-bit portion
one-bit portion
CLK8
shifting clock for 16-bit portion
G4
LK

FIG. 13C


16-bit interval
CLK1
DERR
128-bit interval
YØ
Y4
CON1
128-bit interval
CON2
"HIGH"
CON1
16-bit portion
SØ
16-bit interval
CLK15
G2
LK
G3,G5
16-bit
G4
LK
shifting pulse

AUDIO DATA PROCESSING SYSTEM

DESCRIPTION

The present invention relates to an audio data processing system.

In order to reproduce audio Pulse-Code Modulation (PCM) data, decoding is performed, and then error correction and a compensation are carried out to detect whether or not there is an error.

Conventionally, a Bose-Chaudhuri-Hocquenghem (BCH) error correction circuit performing error corrections on successive samples (64-bit), has been utilised.

Typically, each 64-bit sample is comprised of 56 information bits, 7 error correction bits and 1 redundancy bit, and when an error occurs in the information bits, the error is corrected by use of the error correction bits.

Although the BCH error correction circuit can correct an error of one bit per sample, it cannot correct a so-called "double error" involving 2 or more bits per sample, and instead the BCH error correction circuit outputs a double error signal.

Data for which error correction cannot be performed by the BCH error correction circuit, produces noise. For example, in US Patent No. 4 451 921 entitled, "PCM Signal Processing Circuit" clock noise is produced by a discontinuity of PCM signal data in a wrinkled area or the like of a magnetic tape, and an interpolation to the data situated prior and posterior to the PCM signal data is performed to thereby prevent generation of clock noise in the audio signal.

Though the circuit described in US Patent No. 4 451 921 can prevent noise regenerated in the case of special variable speed regeneration or editing or the like within the audio signal, error correction in the event of the aforesaid double error is not carried out.

As seen from the foregoing, signals which have not undergone double error correction are outputted as noise, which degrades the quality of sound produced from the system.

Accordingly, it is an object of the present invention to provide an audio data processing system which can improve the quality of sound reproduced even during an aforesaid double error in the audio data.

In accordance with the present invention, there is provided an audio data processing system comprising: means for receiving a sequence of digital samples of an audio signal, means for detecting the occurence of double errors (as hereinbefore defined) in samples in the sequence, and means response to said detecting means, to produce an average digital signal, and to substitute said average signal for a detected sample containing a double error, said average signal being based upon an average of values of samples of said audio signal not containing a detected double error, preceding and following said sample containing said double error.

Examples of the invention will now be described with reference to the accompanying drawings in which:

Figure 1 illustrates principle of audio data interpolation, used in the examples of the present invention;

Figure 2 is a block diagram of an audio data interpolating circuit for an audio processing system in accordance with the present invention;

Figure 3 is a detailed block diagram of a data converting unit illustrated in Figure 2;

Figure 4A, 4B and 4C are detailed block diagrams of a pulse generating unit illustrated in Figure 2;

Figure 5 is a detailed block diagram of a data extracting unit illustrated in Figure 2;

Figure 6 is a detailed block diagram of an average value calculating unit illustrated in Figure 2;

Figure 7 is a detailed block diagram of a data selecting unit illustrated in Figure 2;

Figure 8 is a timing digram of a channel grating pulse generating unit illustrated in Figure 4B;

Figure 9 is a timing diagram of a data loading pulse generating unit illustrated in Figure 4C;

Figure 10 is a timing diagram for Figure 2 or Figure 5;

Figure 11 is a timing diagram for Figure 4A during an individual double error occurrence;

Figure 12 is a timing diagram of Figure 4A during a continuous double error occurrence;

Figure 13A is a timing diagram of Figure 5 in a normal condition;

Figure 13B is a timing diagram of Figure 5 during an individual double error occurrence; and

Figure 13C is a timing diagram of Figure 5 during a continuous double error occurrence.

Figure 1A shows a principle of a data interpolation during an individual double error occurrence i.e. when a double error occurs in a single data sample between two non-erroneous samples, whereas Figure 1B is a drawing that shows a principle of data interpolation for a continued double error, i.e. when a double error occurs for two or more successive data samples occuring between non-erroneous samples.

As shown in Figure 1A, in the case of an individual double error (C), the non-erroneous sample data existing prior to (A) and posterior to (B) the erroneous sample data are combined or put together and an average value thereof is used as an interpolation for the value of the data sample (C).

In the case of continued double error as illustrated in Figure 1B, the non-erroneous sample data (A) existing prior to an occurrence of the error is maintained as it is (i.e. for samples C and D), and in

the case of the last double error (E), the non-erroneous sample data existing prior and posterior to the last erroneous data are combined together to thereby get an average value.

In the descriptions that follow, the former case will be called an "average valuation interpolation" and the latter will be called a "pre-interpolation".

In the example of sound data interpolating circuit described hereinafter, the aforementioned average value interpolation and pre-interpolation are performed by the same circuit.

Figure 2 is an overall block diagram of an audio data interpolation circuit for a system in accordance with the present invention.

In Figure 2, a data converting unit 100 converts serial audio data inputted at IN into parallel data samples.

Here, audio data inputted at IN into the data converting unit 100 are supplied from a BCH error correction circuit within a receiving system (not shown).

The BCH error correction circuit receives audio data decoded and outputted by a decoding unit for decoding PCM sound data thereby to perform an error correction, and during a double error occurrence, it outputs a double error signal DERR.

Conventionally, the audio data is a serial stream of 16-bit samples outputted successively in parallel by means of a clock CK 14 generated from a separate clock generating means (not shown).

A pulse generating unit 200 performs a logical combination on the double error signal DERR outputted from the BCH error correction circuit and clock signals (/CK1, CK1-CK7) outputted from the clock generating means to thereby generate interpolating pulses CON1 and CON2, channel gating pulses CHN1-CHN4 and a loading pulse SO.

First, second, third and fourth data extracting units 300-303 have the same construction, and in accordance with interpolating pulses CON1 and CON2 inputted fromthe pulse generating unit 200, channel gating pulses CHN1-CHN4, a loading pulse SO and clock signals (CK1, /CK8, CK13 and CK15) generated from the clock generating means, maintain the non-erroneous data prior to the error occurrence during a double error occurrence, or outputs interpolated data according to the non-erroneous data prior and posterior to the last erroenous sample data.

A data selecting unit 500 outputs data outputted fromthe first, second, third and fourth data extracting units 300-303.

An average value calculating unit 400 derives an average value from the data outputted from the data converting unit 100 and data selecting unit 500 thereby to output the average value to the first, second, third and fourth data extracting units 300-303.

As noted in the foregoing, the audio data interpolating circuit carries out an interpolating process in respect of the double errors which the BCH error correction circuit cannot correct.

Figure 3 is a detailed block diagram of the data converting unit 100 illustrated in Figure 2.

In Figure 2, when a sound data sample inputted to the data converting unit 100 does not contain an individual or a continued error, the double error signal DERR is not generated by the BCH error correction circuit, and a signal of low level is inputted to the pulse generating unit 200.

Accordingly, referring to Figure 4A, a signal of low level is inputted to an input terminal IN of a shift register 201 of an interpolating pulse generating unit in the pulse generating unit 200, and is shifted by a clock (/CK1) as illustrated in Figure 11 thereby to be outputted to ouput terminals Y0-Y7.

Therefore, the signal of low level is ouptutted to the output terminals Y0-Y7 of the shift register 201 to thereby make the first interpolating pulse CON1 outputted by an AND gate 203 a signal of low level and and make a second interpolating pulse CON2 outputted from a NAND gate 204 a signal of high level.

The first and second interpolating pulses CON1 and CON2 are, as shown in Figure 2, respectively inputted to the first, second, third and fourth data extracting units 300-303.

Accordingly, referring to Figure 5, which shows the unit 300 in detail, a signal of low level is outputted from a first AND gate G2 of the data extracting unit (300, or 301 or 302 or 303), and a signal of high level is outputted only in a 16-bit interval which is more delayed by 16 bits than a corresponding channel defined by D flip-flops D1 and D2 and an inverter G1, as illustrated in Figure 13A, so that a clock CLK 13 is outputted from a second AND gate G3.

In other words, as illustrated in Figure 13A, a 16-bit clock CLK 13 which is delayed by more than 16 bits than the corresponding channel, is outputted from the second AND gate G3.

The clock CLK 13 is illustrated in Figure 10.

Therefore, an output of an OR gate G4 becomes the same as the output of the second AND gate G3 to thereby be supplied to clocks of serial and parallel shift registers SPSR1 and SPSR2.

At this point, the clock (/CLK 8) inputted to the serial and parallel shift registers SPSR1 and SPSR2 become high level, as illustrated in Figure 3A, to thereby be enabled.

Accordingly, the serial and parallel shift registers SPSR1 and SPSR2 shift parallel data ADATA outputted from the data converting unit 100 in accordance with the clocks outputted from the OR gate G4 to thereafter output Y the same in series.

Furthermore, because the second interpolating pulse CON2 is a signal of high level, an output of the third AND gate G5 becomes the same as the second AND gate G3 to thereby be supplied to shift registers 310 and 320 as a clock.

The shift registers 310 and 320 shift a serial data outputted from the serial and parallel shift registers SPSR1 and SPSR23 in accordance with the clocks outputted from the third AND gate G5 to thereby output the same as a parallel data BDATA.

As seen from the foregoing, the parallel audio data BDATA outputted from the respective shift registers 310 and 320 of the data extracting unit 300-303 in Figure 2 are respectively inputted to the data selecting unit 500 G10, G20, G30 and G40.

The parallel audio data inputted by bit to respective multiplexers MUX1-MUX16 as illustrated in Figure 7 are selectively outputted to an output terminal D in response to first and second signals generated by first and second NOR gates 510 and 520.

When the double error signal is generated from the BCH error correction circuit as described above, it implies that one sample of the inputted sound data has no error, so the sound data interpolating circuit of the present invention outputs the inputted audio data as it is.

In other words, if the audio data has no error, the inputted data is passed intact without the average value interpolation and pre-interpolation being performed.

Hereinafter, an explanation will be given about how the sound data interpolating circuit performs the average value interpolation and pre-interpolation on the data containing individual or continued double errors.

When an individual double error occurs, the double error signal DERR is outputted during 64-bit interval in the BCH error correction circuit as illustrated in Figure 11.

The double error signal DERR is inputted to the pulse generating unit 200 as illustrated in Figure 2.

At the same time, clocks (/CLK1, CLK2, CLK3, CLK4, CLK5, CLK6 and CLK7) generated fromthe clock generating means are inputted to the pulse generating unit 200 as illustrated in Figures 8 and 9.

An interpolating pulse generating unit of the pulse generating unit 200 generates the first interpolating pulse CON1 as illustrated in Figure 11, in response to an AND gate 203 which performs a logical multiply on an inverted signal of a first output Y0 of the shift register 201 and an inverted signal of a fifth output Y4.

Furthermore, the second interpolating pulse CON2 as illustrated in Figure 11 is generated by an AND gate 204 which performs NAND on a second output Y1 and sixth output Y5 of the shift register 201 of the pulse generating unit 200.

In Figure 11, the interval T represents a 16-bit period in respect of clocking a 64-bit period that contains one complete sample of the audio data.

An interval T1 represents a read time of the audio data and an interval T2 represents an average value interpolating interval in an individual double error.

The average value interpolating interval is a 64-bit interval corresponding to the audio data of one sample.

The channel gating pulse generating unit of the pulse generating unit 200 produces channel gating pulses CHN1, CHN2, CHN3 and CHN4 in accordance with waveforms CLK2, CLK3 and CLK4 as illustrated in Figure 8.

In other words, a demultiplexer 206 shown in Figure 4B sequentially outputs Y0-Y7 pulses of high level in accordance with the waveforms CLK2, CLK3 and CLK4.

First, second, third and fourth OR gates 207-210 which receive the outputs Y0-Y7, when the respective output pulses, Y0 or Y4, Y1 or Y5, Y2 or Y6, Y3 or Y7 are in the high levels, generates the first, second, third and fourth channel gating pulses CHN1, CHN2, CHN3 and CHN4 as illustrated in Figure 8.

A loading pulse generating unit in the pulse generating unit 200 performs a logical multiply on the waveforms CLK5, CLK6, CLK7, CLK1 as illustrated in Figure 9 to thereby generate 16-bit data loading pulses SO.

In other words, the loading pulse generating unit comprised of an AND gate 212 generates loading pulses SO of high level when one of the waveforms CLK5, CLK6, CLK7 and CLK1 is at a high level.

The first and second interpolating pulse CON1 and CON2, the channel gating pulses CHN1, CHN2, CHN3 and CHN4, and loading pulses SO outputted from the pulse generating unit 200 are respectively inputted into the first, second, third and fourth data extracting units 300, 301, 302 and 303.

The reason there are 4 channel gating pulses CHN1, CHN2, CHN3 and CHN4 as illustrated in Figure 8 is that the data audio signals are for a television satellite broadcast system and there exist 4 channels within each audio data sample in the PCM transmitting method for a conventional television satellite broadcasting system. However, it will be appreciated that a different number of channel gating pulses CHN can be provided depending upon the number of audio channels.

In the case of 4 channels, the bit number of audio data corresponding to one channel within one data sample becomes 16 bits.

Therefore, the data converting unit 100 as illustrated in Figure 2 receives 16-bits of audio data serially.

The data converting unit 100, as illustrated in Figure 3, comprises two 8-bit shift registers 101 and 102 corresponding to a 16-bit shift register.

The data converting unit 100 converts the inputted serial audio data to 16-bit parallel audio ADATA in response to a clock CLK14 as illustrated in Figure 10 thereby to output the same.

The 16-bit parallel audio data ADATA outputted from the data converting unit 100 is inputted in parallel to the average value calculating unit 400 and at the same time, is inputted to respective input terminals SER of the first, second, third and fourth data extracting unit 300-303.

At this moment, the 16-bit parallel sound data ADATA is inputted to a parallel port of the average value calculating unit 400 and inputted to a serial port of the first, second, third and fourth data extracting units 300, 301, 302 and 303.

Also, the respective serial ports of the data extracting units 300, 301, 302 and 303 are connected to only one line of the data output ADATA which receives the uppermost bit of 16-bit parallel audio data ADATA outputted from the data converting unit 100.

The data extracting units 300, 301, 302 and 303 have respective constructions as illustrated in Figure 5 and for convenience sake, the first data extracting unit 300 will be explained in detail.

In Figure 5, a clock signal CLK5 illustrated in Figure 10 is fed to input terminal of the first AND gate G2.

A clock signal CLK 13 illustrated in Figure 10 is inputted to one input ternal of the second AND gate G3.

A clock (/CLK8) as illustrated in Figure 13B which is an inverted clock CLK8 as illustrated in Figure 10, is inputted to load terminals LD of the shift registers SPSR1 and SPSR2, shown in Figure 5.

The data inputted to parallel input terminals SDATA of the shift registers SPSR1 and SPSR2 is 16-bit parallel data fedback from the average value calculating unit 400 and 16-bit parallel data which is prior by one sample data to the currently-inputted channel data.

The first and second interpolating control signals, the first channel gating signal and loading signal are inputted to respective input terminals of the signal generating unit 200.

Accordingly, waveforms outputted from an OR gate G4 become the same as those G4 illustrated in Figure 13B.

If the above waveforms are compared with the waveforms G4 of Figure 13A, which are the first clock pulses under normal state where the double error has not occurred, it can be noted that loading clock pulse LK has been added to the clock for shifting the 16-bit data.

When the clock (/CLK8) inputted to the load terminals LD of the shift registers SPSR1 and and SPSR2 is low as illustrated in Figure 13B, the shift registers SPSR1 and SPSR2 load 16-bit parallel data SDATA outputted from the average value calculating unit 400 in accordance with the loading pulses outputted from the OR gate G4.

Henceforth, when the clock (CLK8) inputted into the load terminals LD is high level, shifted data are outputted to an output terminal Y of the shift register SPSR2 in the order of SDATA15, SDATA14, SDATA13, ..., SDATA0 in response to a 16-bit shift clock outputted from the OR gate G4.

When the 16-bit data inputted from the average value calculating unit 400 are sequentially outputted, data for each successive channel is outputted by repeated performances of the aforementioned operations.

In the foregoing descriptions, an explanation was given only to one channel for convenience sake. However the interpolating operation is performed on the data of the sample.

In other words, as depicted in Figure 11, the high level interval for the first interpolating pulse CON1 is 64-bit interval, however, for convenience sake, an explanation was given on the 16-bit interval only.

Accordingly, the loading clock LK and shifting clock described in Figure 13B, are generated repeatedly for each of the channels.

As seen from the foregoing, when the 16-bit data of the last channel out of the data inputted from the average value calculating unit 400 is outputted, data outputted from the data converting unit 100 is sequentially inputted to an input terminal SI of the shift register SPSR1.

The data outputted from the data converting unit 100 and inputted to the input terminal SI of the shift register SPSR1 is also shifted thereby to be outputted.

As seen from the foregoing, the respective data extracting units 300, 301, 302 and 303 selectively output bits (16-bit) corresponding to one channel out of the sample data (64-bit) in accordance with channel gating pulses CHN1, CHN2, CHN3 and CHN4 outputted from the pulse generating unit 200.

Here, as depicted in Figure 11 the reason the first interpolating pulse CON1 is made to be interpolated within the interval T2 of high level is because a data read time as much as the interval T1 is needed.

Serial 16-bit data out putted at terminal Y from the shift register SPSR2 is inputted at terminal A to a shift register 320.

The shift register 320 converts the data inputted serially in response to the clock outputted from a third AND gate G5, into parallel data, thereby to output the same.

The uppermost bit outputted from the shift register 320 is serially inputted at A into shift register 310. The shift registers 310 and 320 have 8-bit output ports, which correspond to a 16-bit shift register.

Accordingly, 16-bit parallel audio data for the respective channels are respectively inputted to parallel input terminals G10, G20, G30 and G40 of a

data selecting unit 500 for selecting data in response to the sound channels.

The detailed construction of the data selecting unit 500, as illustrated in Figure 7, comprises 4 input multiplexers MUX1-MUX16.

Outputs of NOR gates 510 and 520 for inputting channel gating pulses (CHN1, CHN2) and (CHN1, CHN3) are inputted to respective selective terminals SO and SI of the multiplexers MUX1-MUX16.

As seen from the above, it is apparent that the data selecting unit 500 can automatically select amongst the 4 channels without the assistance of the fourth channel gating pulse CHN4.

The data selecting unit 500 outputs the inputted 16-bit parallel data to an output terminal D in an input order of the channel data.

The data outputted from the data selecting unit 500 is inputted to the average value calculating unit 400. The average value calculating unit 400 produces average value from the data BDATA inputted from the data selecting unit 500 and the data ADATA inputted from the data converted unit 100. Thus, in the case of individual double error as explained in the above, an average value interpolation is performed according to principle described with reference to Figure 1A.

In Figure 1A, in the case of an individual double error, the data prior and posterior to the individual double error are combined, then divided by 2, and the data thus obtained is outputted.

In the average value calculating unit 400 as illustrated in Figure 6, two inputs in the uppermost bit of the input terminals A3 and B3 of an adder ADD1 are inverted by inverters IN1 and IN2 to thereby be added, and the other balance bit inputs are one another corresponded to thereby be added.

Then, an output from an output terminal CO of the uppermost bit of the adder ADD1 is inverted by an inverter IN3, so that an average value of the two inputs is produced at the output terminal SDATA.

The average value calculating unit 400, as explained in the foregoing, processes in channel order, 16 bit channel samples outputted from the data selecting unit 500, and the processed outputs are supplied to the input terminals SDATA of the data extracting units 300, 301, 302 and 303.

Accordingly, the shift registers SPSR1 and SPSR2 as illustrated in Figure 5, load the average value-interpolated 16-bit parallel data when the clock (/CLK8) inputted into the load terminal LD is low and a loading pulse LK illustrated in Figure 13B is inputted.

Then, the data loaded into the shift registers SPSR1 and SPSR2 are shifted in response to the 16-bit shift clock to thereby be outputted in series.

The shift registers 310 and 320 convert the data outputted from the shift registers SPSR1 and SPSR2 to parallel data to thereby output the same BDATA.

Accordingly, the data selecting unit 500 responds to the channel gating pulses CHN1, CHN2 and CHN3 thereby to output in parallel the average value-interpolated 64-bit data in units of 16 bits.

The average value-interpolated and outputted parallel audio data are generally converted again to analog audio signals to be outputted thereafter through a speaker and the like, and the output has an improved tone quality as compared with the double error-ridden sound data outputted without correction.

An explanation of a pre-interpolation performed during a continued double error, will now be given.

In the case of the continued double error, the double error signal DERR outputted from the BCH error correction circuit is maintained at a high level for a

128-bit interval (64-bit x 2), as illustrated in Figure 12.

Accordingly, the first interpolating pulse CON1 maintains a high level state for a period during which double error signal DERR is transmitted.

Furthermore, the second interpolating pulse CON2 maintains a low level for an interval T2, and thereafter maintains a high level.

In Figure 12, the interval T1 represents a data read time and T3 represents an interpolating time.

Accordingly, as illustrated in Figure 5, operational waveforms of the data extracting unit 300 are represented as in Figure 13C.

The first AND gate G2 does not produce the loading clock pulse LK until after the first 128-bit interval following the double error signal DERR becoming high, but the gate produces the loading clock for the balance 128-bit interval.

It can be noted that, in the 128-bit interval where the continued double error has occurred, the loading clock is produced every 16-bit interval, bringing the number of the clock pulses to 8.

In Figure 13C, however, for convenience sake, an interval corresponding to 16 bits is illustrated.

The pulses outputted from the third AND gate G5 during the interval T2 of the second interpolating pulse CON2 as illustrated in Figure 12 maintain the previously-inputted sample data, and the average value interpolating operations are, as mentioned before, performed in the average value calculating unit 400 during the next sample period.

The reason a difference of 16 bits occurs between the interval T1 and the interval T2 in Figure 12 is because there exists a difference of 16 bits against the data generated between the shift registers (SPSR1, SPSR2) and the shift registers (310, 320) of Figure 5.

As seen from the foregoing, the present invention has an effect of improved tone quality as a result of processing by interpolation the sound data wherein individual and continued double errors uncorrectable by means of the error correction circuit have occurred.

Although the invention has been described in detail with reference to its presently preferred embodiments, it will be understood by one of ordinary skill in the art that various modifications can be made, without departing from the scope of the invention defined in the appended claims.

CLAIMS

1. An audio data processing system comprising:

means for receiving a sequence of digital samples of an audio signal;

means for detecting the occurence of double errors (as hereinbefore defined) in samples in the sequence; and

means response to said detecting means, to produce an average digital signal, and to substitute said average signal for a detected sample containing a double error, said average signal being based upon an average of values of samples of said audio signal not containing a detected double error, preceding and following said sample containing said double error.

2. A system according to claim 1 wherein in response to a detected single occurrence of a sample containing a double error, the value of said average signal is based upon the values of the samples immediately preceding and following the detected sample containing the error.

3. A system according to claim 1 wherein in response to a detected succession of samples containing a double error, at least a first of said double error containing samples is substituted by a value based upon the value of a preceding sample detected not to contain a double error.

4. A system according to claim 3 including means responsive to the detection of said succession of samples containing double errors, to substitute said average signal for at least the last sample in the succession, and to substitute the value of a signal detected not to contain a double error that occurred prior to said succession, for the remainder of the samples of the succession.

5. A system according to claim 3 or 4 including a data extracting unit to receive the digital audio samples successively, an average value calculating circuit to calculate said average value, and a data selecting unit operative to output said received samples in the event of no detected double error, to output said average value in the event of a single

occurrence of a double error between samples that are detected to contain no double errors, and to output more than once the last sample not containing a double error and then said average value in response to a succession of detected samples containing detected double errors.

6. A system according to any preceding claim wherein said detecting means comprises a BCH correction circuit which corrects single digital errors and provides a predetermined output in response to double errors.

7. A system according to any preceding claim wherein said samples each contain data concerning a plurality of audio channels, and including multiplexer means for producing said average signal in respect of the data for each said channel respectively based upon the corresponding data for each channel in said samples preceding and following the detected sample containing the double error.

8. A system according to any preceding claim including converting means to receive a serial digital audio data stream and to convert said stream into multi-bit parallel samples, whereby to provide said digital sample sequence.

9. A sound data interpolating circuit, comprising: data converting means for converting an inputted serial sound data to a parallel sound data to thereby output the same; pulse generating means for generating interpolating pulses, channel gating pulse and loading pulses according to a double error signal outputted from the BCH error correction circuit and a clock signal generated from clock generating means; data extracting means for maintaining a prior data during a double error occurrence or outputting a data interpolating pulses inputted from the pulse generating means, channel gating pulses, loading pulses and clock signal generated from the clock generating means; data selecting means for outputting data outputted from the data extracting means according to a sound channel; and average value calculating means for striking an average from the data outputted from the data converting means

and data selecting means to thereafter output the average value.

10. A sound data interpolating circuit as defined in claim 9, wherein the sound data inputted to the data converting means is the data which has performed the error correction at the BCH error correction circuit.

11. A sound data interpolating circuit as defined in cliam 1 or claim 2, wherein the BCH error correction circuit inputs a sound data decoded and outputted by a decoding unit for decoding a PCM-coded sound data to thereby perform an error correction and simultaneously outputs the double error signal during an occurrence of double error.

12. A sound data interpolating circuit as defined in claim 9, wherein the data converting means converts a serially-inputted sound data to a 16-bit parallel data tp thereafter output the same.

13. A sound data interpolating circuit as defined in claim 9, wherein the data converting means comprises a first shift register for shifting a serially-inputted sound data to thereby oupt the same in an 8-bit parallel data; and a second shift register for using the uppermost bit as an input out of the parallel data shifted and outputted from the first shift register to thereafter output the same in an 8-bit parallel data.

14. A sound data interpolating circuit as defined in claim 9, wherein the pulse generating means comprises an interpolating pulse generating unit for generating interpolating pulses from the double error signal outputted from the BCH error correct circuit; a channel gating pulse generating unit for generating channel gating pulses in accordance with the sound data channel; and a loading pulse generating unit for generating loading pulses in order to output a 16-bit data interpolated during an occurrence of double error.

15. A sound data interpolating circuit as defined in claim 14, wherein the interpolating pulse generating unit comprises: a shift register for shifting the

double error signal inputted from the the BCH error correction circuit in response to a clock generated fromthe clock generating means; and a AND gate for generating a first interpolating pulse by perofrming a logical multiply on a signal outputted from a first output termianl of the shift register and then inverted from an inverter and a signal outputted from a fourth output terminal of the shift register; and a NAND gate for perofrming a logical multiply on signals outputted from a second and a fifth output terminal to thereby invert the same, so that a second interpolating pulse can be generated.

16. A sound data interpolating circuit as defined in claim 15, wherein a clock generated from the clock generating means has a pulse width corresponding to a 16-bit serial sound data.

17. A sound data interpolating circuit as defined in claim 14, wherein a channel gating pulse generating unit comprises demultiplexers for generating pulses in response to a clock outputted from the clock generating means; and a logic gate for ouptutting

channel gating pulses by performing a logical sum on pulses outputted from the demultiplexers.

18. A sound data interpolating circuit as defined in claim 17, wherein the clock outputted from the clock generating means has pulse widths corresponding to 32-bit, 64-bit and 128-bit serial sound data.

19. A sound data interpolating circuit as defined in claim 17, wherein the channel gating pulse has the same number as the channle number and a pulse width corresponding to an interval where one sample interval is deivided by the channel number.

20. A sound data interpolating circuit as defined in claim 14, wherein the loading pulse generating unit comprises AND gates for performing a logical multiply on the clock generated from the clock generating means.

21. A sound data interpolating circuit as defined in claim 20, wherein the clock generated from the clock generating means have clock numbers corresponding to a

result where bit numbers of one channel are divided by 2, 4, 8 and 16.

22. A sound data interpolating circuit as defined in claim 9, wherein the data extracting means comprises a clock control unit for generating a data shifting clock encompassing loading pulses in response to an occurrence of double error; a data selecting unit for selectively outputting data shifting clocks including loading pulses generated from the clock control unit and data interpolated or inputted by a clock having a pulse width corresponding to one bit; and a data outputted from the data selecting unit to thereby output the same in parallel.

23. A sound data interpolating circuit as defined in claim 22, wherein the clock control unit comprises: a first AND gate for performing a logical multiply on a clock for generating one pulse per data bit, a first interpolating pulse generated from the interpolating pulse generating unit, a clock gor generating one pulse per channel and the first channel gating pulse; a demultiplexer for delaying by a period corresponding to

one channel the first channel gating pulse in response to a clock having a pulse width corresponding to a 16-bit interval of the data; a second AND gate for performing a logical multiply on the first channel gating pulse delayed by the demultiplexer and a clock for generating a pulse per data; an OR gate for performing a logical multiply on the first and second AND gates to thereby generate data shifting clocks including loading pulses; and a third AND gate for performing a logical multiply onthe output of the second AND gate and the second interpolating signal to thereby generate a clock for shifting a data corresponding to one channel.

24. A sound data interpolating circuit as defined in claim 22, wherein the data selecting unit includes a shift register for loading a clock having a pulse width corresponding to one bit and a signal interpolated from the average value calculating means by the loaidng pulses outputted from the clock control unit, and for shifting a data loaded by a data shifting clock outputted from the clock control unit and a sound

data inputted from the data converting unit, to thereby output the same in series.

25. A sound data interpolating circuit as defined in claim 22 wherein the data outputting unit shifts the data outputted from the data selecting unit in response to the clock outputted from the clock control unit to thereby output the same as parallel data.

26. A sound data interpolating circuit as defined in claim 9, wherein the data selecting means includes multiplexers for outputting sequentially, in parallel and by channel the data inputted from the data extracting means in response to gating pulses generated from the gating pulse generating unit.

27. An audio data processing system substantially as hereinbefore described with reference to the accompanying drawings.

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Databases (see over)

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Documents considered relevant following a search in respect of claims 1 TO 27

Category (see over)	Identity of document and relevant passages	Relevant to claim(s)
A	US 4430736 (SCHOLZ) see column 2 line 45 to column 6 line 3	

Category	Identity of document and relevant passages	Relevant to claim(s)

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